11. (Amended) The device of claim 10, wherein the anisotropic conductive film prevents oxygen and moisture from permeating through the second insulating substrate.

25. (New) The organic EL device of claim 6, wherein the conductive bump pad is directly connected to the metal electrode with a conductive bonding agent.

Remarks

Reconsideration of this Application is respectfully requested in light of the foregoing amendments and the following remarks because entry of these amendments place the application in condition for allowance. It is believed that the amended claims do not add new matter to the application and are fully supported by the specification as filed. Specification has been amended to correct the minor informalities and grammatical errors.

Claims 1- 25 are pending, among which claims 13-24 were not elected for prosecution subject to the restriction requirement. Among the claims 1-12 and 25 that are being considered, claims 1, 6 and 9 are independent claims.

Attached hereto is a marked-up version of the changes made by the current amendment. The attachment is captioned "Version with Markings to Show Changes Made".

Rejections Under 35 U.S.C. § 112:

On page 2 of the Office Action, the Examiner rejected claims 2-5 under 35 U.S.C. § 112 for minor informalities. Claim 2 has been amended to correct such informalities. Objections

over claims 3-5 also appear to be being dependent from the objectionable claim. Therefore, it is respectfully requested that all the outstanding objections and rejections over claims 2-5 be withdrawn and pass those claims to allowance.

Rejections Under 35 U.S.C. § 102:

On page 3 of the Office Action, the Examiner rejected claims 1 and 6-12 under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,215, 244 issued to Kuribayashi *et al.* ("Kuribayashi")

The Examiner alleges that Kuribayashi discloses all the elements recited in the claim 1, referring to Figs. 5 and 13-17. However, the newly amended claim 1 recites an organic EL device, comprising a thin film transistor (TFT) array substrate including a first insulating substrate, a TFT with a conductive interface pad connected thereto and a capacitor formed on the first insulating substrate; and an organic EL substrate including a second insulating substrate, a transparent electrode, an organic EL layer and a metal electrode, wherein the conductive interface pad is directly connected to the metal electrode. Kuribayashi neither discloses nor suggests such features. Therefore, newly amended claim 1 is patentable over Kuribayashi. Likewise, claims 2-5 that are dependent from the newly amended claim 1 are also patentable over Kuribayashi.

Bridging from page 3 to 4 of the Office Action, the Examiner rejected claims 6, 9, 8 and 11 under 35 U.S.C. § 102 as being anticipated by Kuribayashi, providing individual grounds for rejection. However, claim 6 has been amended, reciting an organic EL device, comprising: a thin film transistor (TFT) array substrate including a first insulating substrate, a TFT with a

conductive interface pad connected thereto, a capacitor formed on the first insulating substrate and a conductive bump pad formed on the conductive interface pad; and an organic EL substrate including a second insulating substrate, a transparent electrode, an organic EL layer and a metal electrode, wherein the conductive bump pad is directly connected to the metal electrode. Kuribayashi neither discloses nor suggests such features. Likewise, claims 7, 8 and 25 that are dependent from the amended claim 6 are also patentable over Kuribayashi. Therefore, those claims of 6-8 and 25 are also patentable over Kuribayashi.

Similarly, claim 9 has been amended and now recites an organic EL device, comprising: a thin film transistor (TFT) array substrate including a first insulating substrate, a TFT, a capacitor formed on the first insulating substrate, a conductive interface pad and a conductive bump pad formed on the conductive interface pad; and an organic EL substrate including a second insulating substrate, a transparent electrode, an organic EL layer and a metal electrode, and a polymer bump, wherein the conductive bump pad contacts a portion of the metal electrode corresponding to the polymer bump by a conductive bonding agent, and wherein the TFT is electrically connected to the metal electrode.

Kuribayashi neither discloses nor suggests such features. Likewise, claims 10-12 that are dependent from claim 9 are also patentable over Kuribayashi

On page 4 of the Office Action, the Examiner further rejected claims 1 and 12 under 35 U.S.C. as being anticipated by U.S. PG-Pub 2001/0011868 of Fukunaga *et al.* ("Fukunaga").

The Examiner alleges that Fukunaga discloses in Figs. 4 and 5 an organic EL device, comprising a thin film transistor (TFT) array substrate including a first insulating substrate, a TFT 401/402 and a capacitor 504 formed on the first insulating substrate; and an organic EL

substrate including a second insulating substrate, a transparent electrode, an organic EL layer 331/332 and a metal electrode 326.

As discussed previously, the newly amended claim 1 recites an organic EL device, comprising a thin film transistor (TFT) array substrate including a first insulating substrate, a TFT with a conductive interface pad connected thereto and a capacitor formed on the first insulating substrate. Fukunaga neither discloses nor suggests such a feature. Therefore, the amended claim 1 is patentable over Fukunaga and claim 12 that is dependent from the amended claim 1 is also patentable over Fukunaga.

Furthermore, Fukunaga does not disclose an organic EL substrate including a second insulating substrate, a transparent electrode, an organic EL layer and a metal electrode. In Fukunaga, a transparent electrode and an organic EL layer are formed on the so called element-forming substrate. (*See* Figs. 2A, 2B, 4C, 4D and 6. Also *see* paragraphs 0066 through 0071 of Fukunaga) Therefore, Fukunaga does not disclose an organic EL substrate as recited in the claim of the present Application.

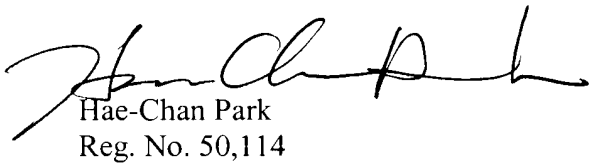
As such, it is respectfully submitted that claims 1-12 and 25 are now patentable over the references of record and requested to withdraw all the outstanding rejections and objections over claims 1-12 be withdrawn and pass claims 1-12 and 25 to issuance.

Conclusion

Applicant respectfully submits that the foregoing remarks demonstrate that entry of these amendments places the present application in condition for allowance. All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,



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October 31, 2002

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Version with Markings to Show Changes Made

In the title:

Please amend the title of the invention to read as follows: – Organic EL Device –.

In the Specification:

Please enter the following amendments.

On page 8, lines 12-21, please replace the paragraph with the following:

Thereafter, a first metal layer is deposited on the gate insulating layer 420 using, for example, a sputtering technique to a predetermined thickness. The first metal layer comprises a metal such as aluminum (Al) and aluminum-neodymium alloy (Al:Nd). As shown in Figs. 5, 6 and 19 the first metal layer is patterned to form a first gate electrode 120 of the first TFT 100, a second gate electrode 220 of the second TFT 200, a first capacitor electrode 310 of the storage capacitor 300, and a gate line 430. Subsequently, an n-type or a p-type impurity is ion-implanted into the first and second semiconductor layers 110 and 220 to form a first source region 130 and a first drain region 140 of the first TFT 100 and a second source region 240 [source] and a second drain region 230 of the second TFT 200.

Please replace the paragraph bridging from page 8, line 22 to page 9, line 12 with the following:

In more detail, on a portion of the gate insulating layer 420 corresponding to the

first semiconductor layer 110, the first gate electrode 120 having an area size smaller than the first semiconductor layer 110 is formed. The gate line 430 is arranged in a transverse direction spaced apart from the first semiconductor layer 110 and is connected to the first gate electrode 120. At this point, the first semiconductor layer 110 includes the source region 130 and the drain region [and] 140, respectively, formed on both end portions thereof. The first capacitor electrode 310 is formed between the first gate electrode 120 and the second gate electrode 220 in such a way that it is spaced apart from the drain region 140 of the first semiconductor layer 110 and is connected to the second gate electrode 220. On a portion of the gate insulating layer 420 corresponding to the second semiconductor layer 210, the second gate electrode 220 having a smaller area size than the second semiconductor layer 210 is formed. At this point, the second semiconductor layer 210 includes the drain region 230 and the source region 240, respectively, formed on both end portions thereof.

On page 10, lines 6-11, please replace the paragraph with the following:

Subsequently, a second metal layer is deposited on the interlayer insulator 440 using, for example, a sputtering technique. As shown in Figs. 11, 12 and 19, the second metal layer is patterned to form a first source electrode 182 and a <u>first</u> [second] drain electrode 184 of the first TFT 100, a second source electrode 282 and a second drain electrode 284 of the second TFT 200, a second capacitor electrode 330 of the storage capacitor 300, a data line 450, and a common power line 460.

On page 13, lines 12-15, please replace the paragraph with the following:

The TFT array substrate 500 of Fig. 21 is assembled with an [a] organic EL substrate 600 in Fig. 25. Figs. 22, 23, 24 and 25 are cross-sectional views illustrating a process of manufacturing the organic EL substrate 600 according to the second preferred embodiment of the present invention.

In the Claims:

Please delete claim 2 without any disclaimer and a prejudice to and amend claims 1, 3, 6-9 and 11 as follows and add a new claim 25.

1. (Amended) An organic EL device, comprising:

a thin film transistor (TFT) array substrate including a first insulating substrate, a TFT with a conductive interface pad connected thereto and a capacitor formed on the first insulating substrate; and

an organic EL substrate including a second insulating substrate, a transparent electrode, an organic EL layer and a metal electrode,

wherein the conductive interface pad [TFT] is directly [electrically] connected to the metal electrode.

3. (Amended) The device of claim 1 [2], wherein the organic EL substrate further includes a protection film that prevents external oxygen and moisture from permeating.

6. (Amended) [The device of claim 1, wherein the TFT array substrate further includes a conductive interface pad connected to the TFT and a conductive bump pad formed on the conductive interface pad, the conductive bump pad contacting the metal electrode of the organic EL substrate by a conductive bonding agent] An organic EL device, comprising:

a thin film transistor (TFT) array substrate including a first insulating substrate, a TFT with a conductive interface pad connected thereto, a capacitor formed on the first insulating substrate and a conductive bump pad formed on the conductive interface pad; and

an organic EL substrate including a second insulating substrate, a transparent electrode, an organic EL layer and a metal electrode,

wherein the conductive bump pad is directly connected to the metal electrode.

7. (Amended) The organic EL device of claim 25 [6], wherein the conductive bonding agent is an anisotropic conductive film (ACF).

8. (Amended) The organic EL device of claim 7, wherein the anisotropic conductive film prevents [serves to prevent] external oxygen and moisture.

9. (Amended) [The device of claim 1, wherein the TFT array substrate further includes a conductive interface pad and a conductive bump pad formed on the interface pad, and the organic EL substrate further includes a polymer bump, wherein the conductive bump pad contacts a portion of the metal electrode corresponding to the polymer bump by a conductive bonding agent.] An organic EL device, comprising:

a thin film transistor (TFT) array substrate including a first insulating substrate, a TFT, a capacitor formed on the first insulating substrate, a conductive interface pad and a conductive bump pad formed on the conductive interface pad; and

an organic EL substrate including a second insulating substrate, a transparent electrode, an organic EL layer and a metal electrode, and a polymer bump,

wherein the conductive bump pad contacts a portion of the metal electrode corresponding to the polymer bump by a conductive bonding agent, and

wherein the TFT is electrically connected to the metal electrode.

11. (Amended) The device of claim 10, wherein the anisotropic conductive film prevents [serves to prevent] oxygen and moisture from permeating through the second insulating substrate.

25. (New) The organic EL device of claim 6, wherein the conductive bump pad is directly connected to the metal electrode with a conductive bonding agent.

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